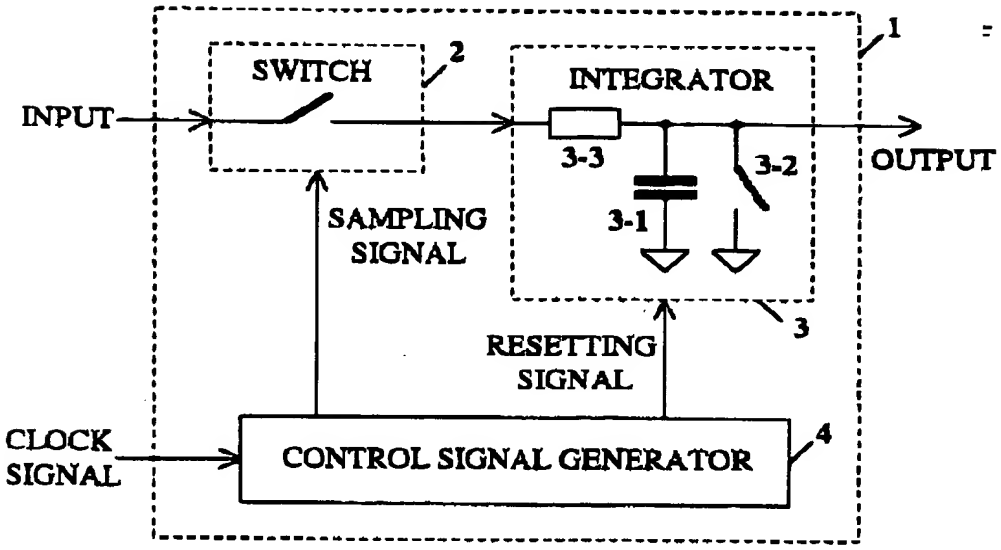


FIG. 1A

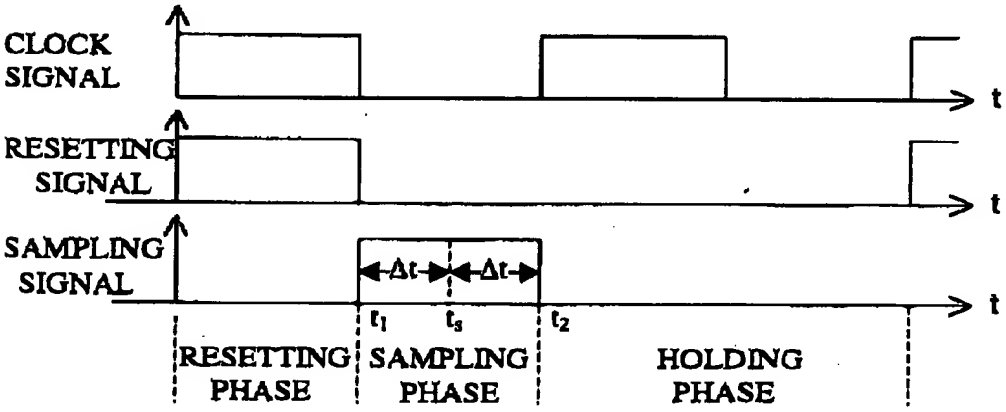


FIG. 1B

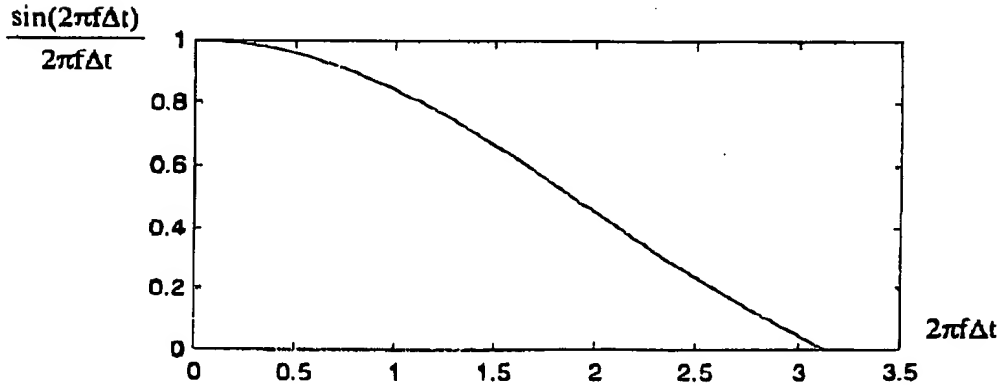


FIG. 1C

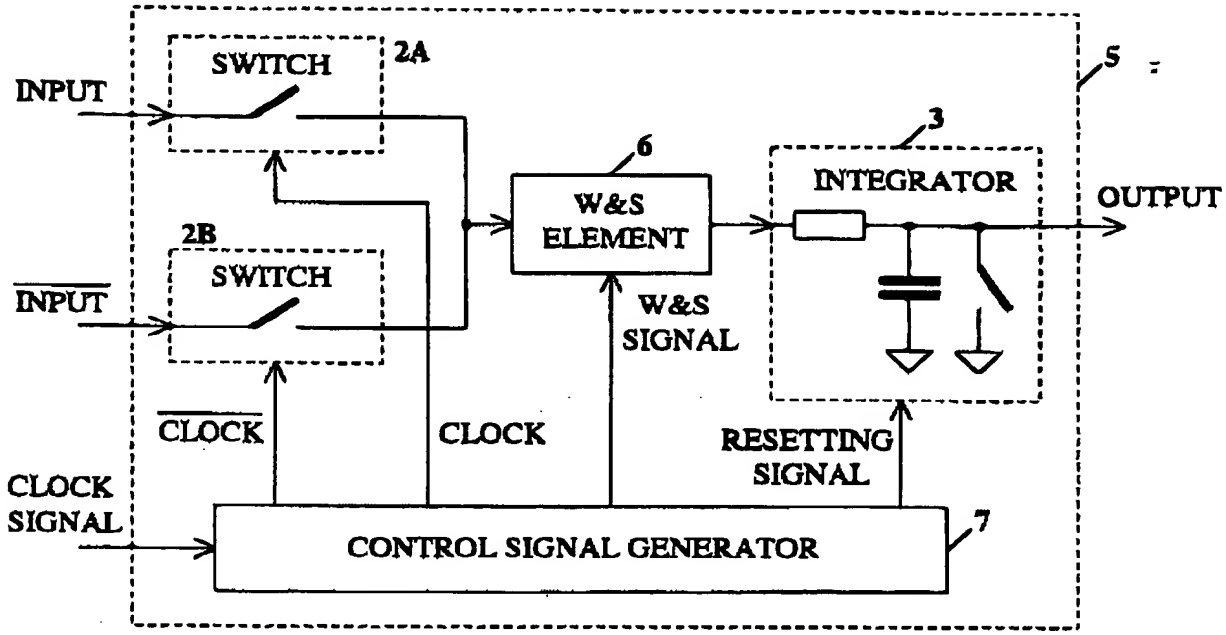

INPUT
SWITCH
2A
5
3
6
INTEGRATOR
OUTPUT
W&S
ELEMENT
2B
SWITCH
INPUT
W&S
SIGNAL
CLOCK
CLOCK
RESETTING
SIGNAL
CLOCK
SIGNAL
CONTROL SIGNAL GENERATOR
7

FIG. 2A

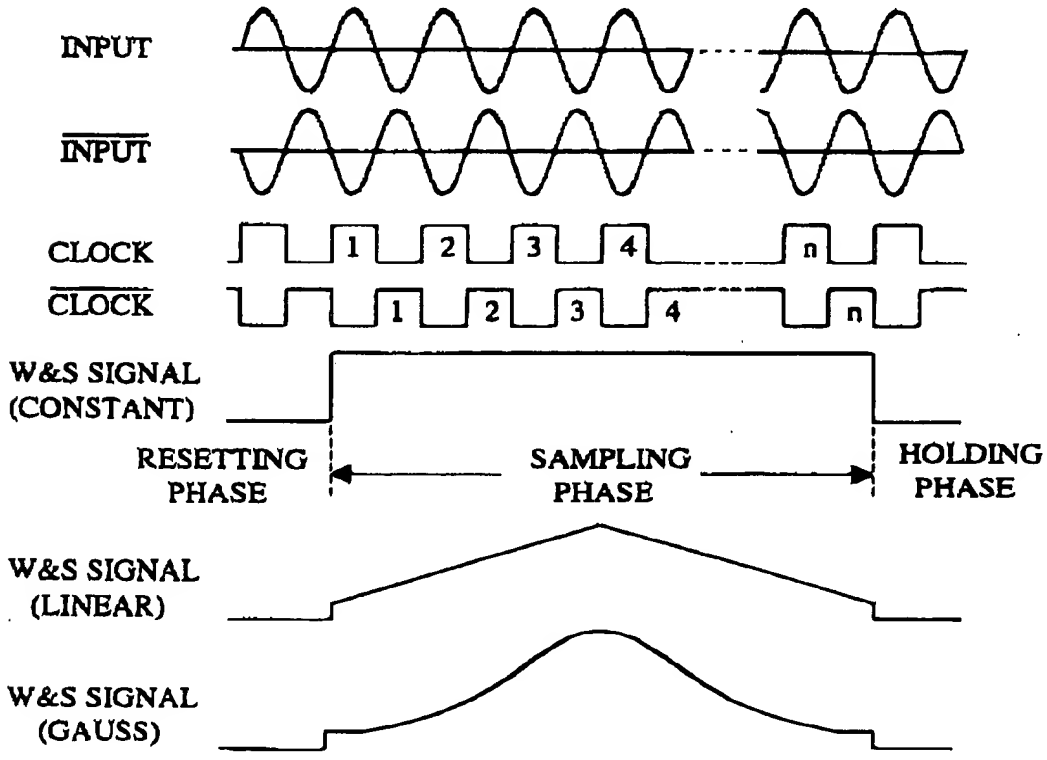

INPUT
INPUT
CLOCK
1
2
3
4
n
CLOCK
1
2
3
4
n
W&S SIGNAL
(CONSTANT)
RESETTING
PHASE
SAMPLING
PHASE
HOLDING
PHASE
W&S SIGNAL
(LINEAR)
W&S SIGNAL
(GAUSS)

FIG. 2B

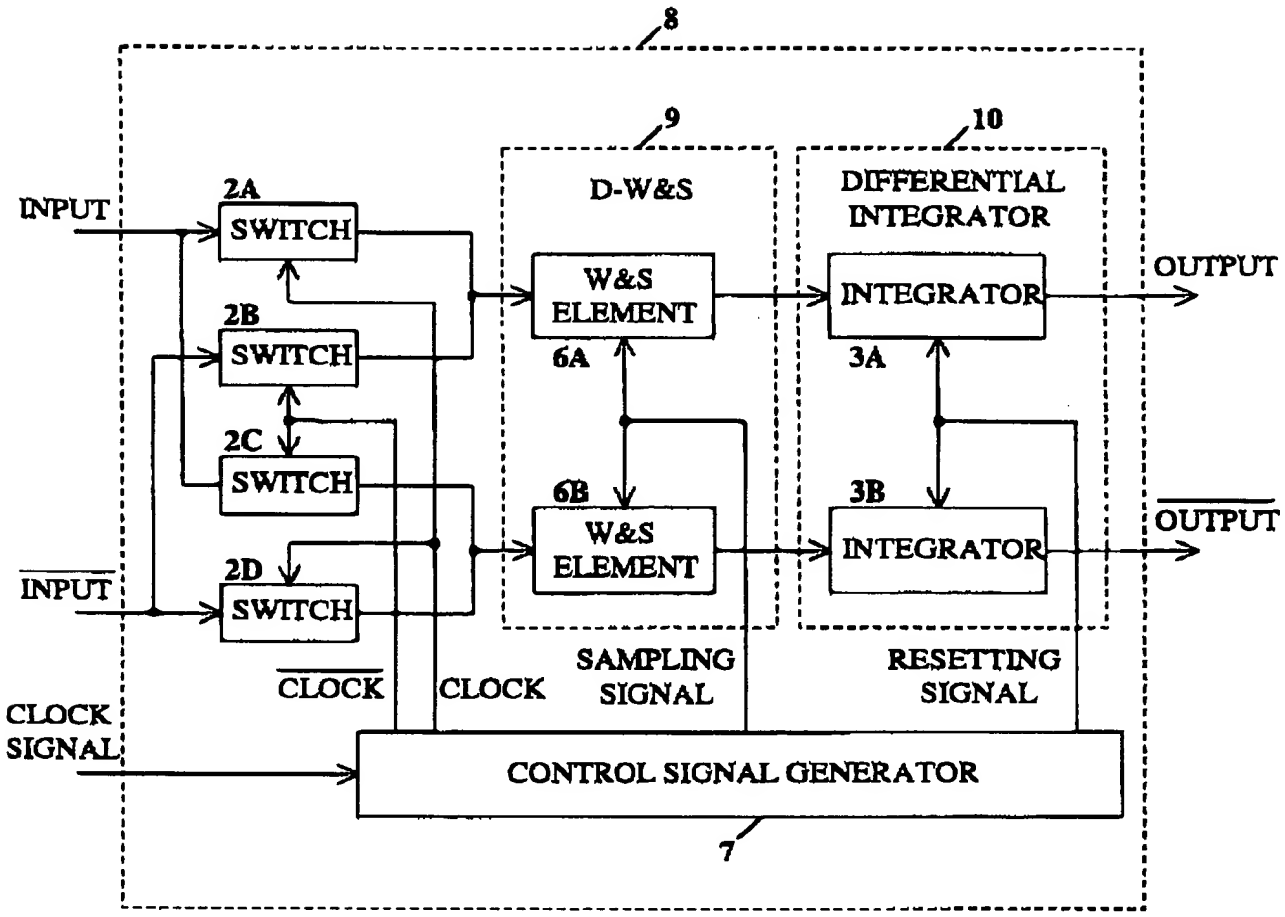

8
9
10
D-W&S
DIFFERENTIAL INTEGRATOR
INPUT
2A
SWITCH
2B
SWITCH
2C
SWITCH
2D
SWITCH
W&S ELEMENT
6A
6B
W&S ELEMENT
INTEGRATOR
3A
3B
INTEGRATOR
OUTPUT
OUTPUT
INPUT
CLOCK
CLOCK
SAMPLING SIGNAL
RESETTING SIGNAL
CLOCK SIGNAL
CONTROL SIGNAL GENERATOR
7

FIG. 3

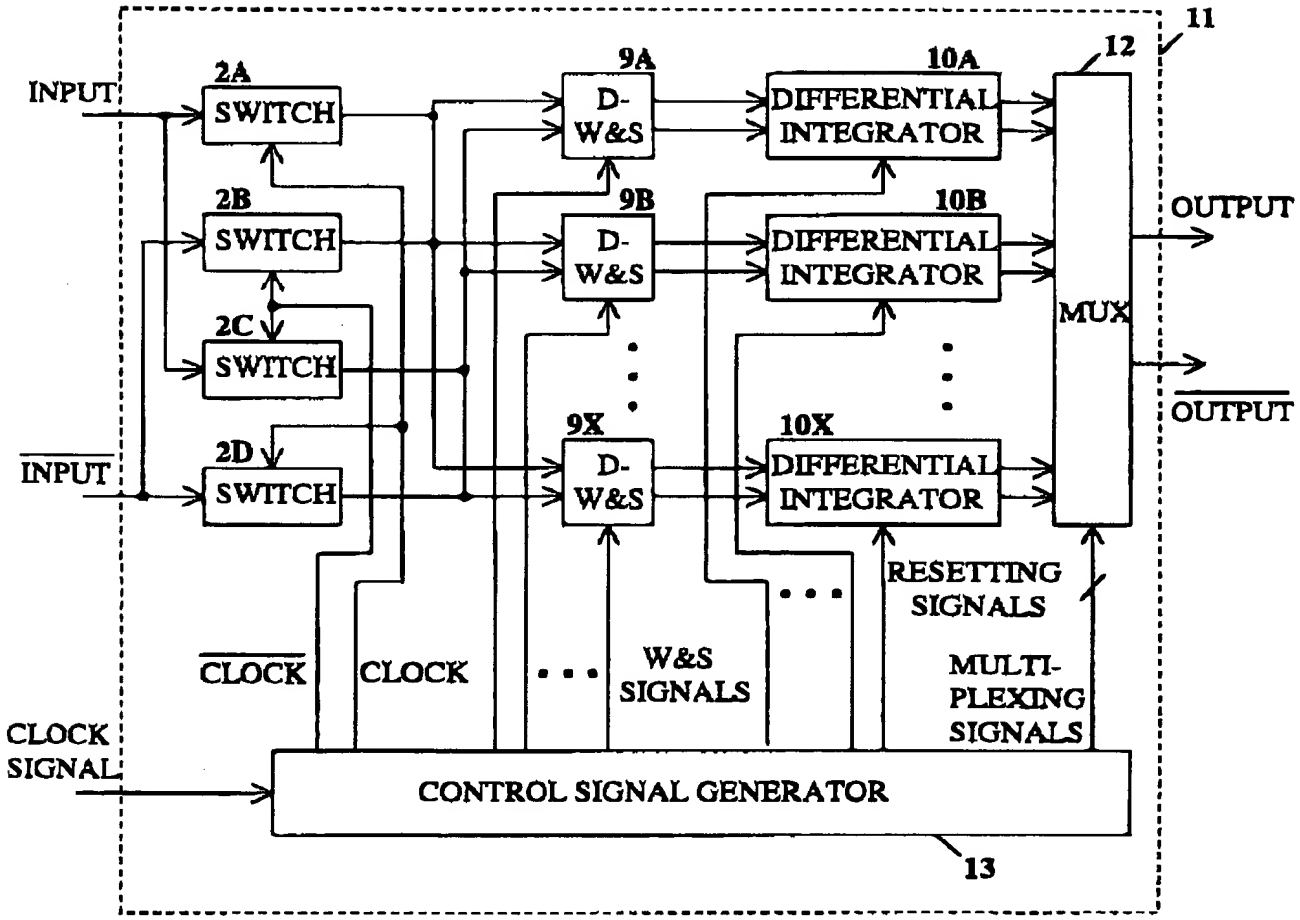

11
12
INPUT
2A
SWITCH
9A
D-
W&S
10A
DIFFERENTIAL
INTEGRATOR
2B
SWITCH
9B
D-
W&S
10B
DIFFERENTIAL
INTEGRATOR
OUTPUT
2C
SWITCH
MUX
9X
10X
INPUT
2D
SWITCH
D-
W&S
DIFFERENTIAL
INTEGRATOR
OUTPUT
RESETTING
SIGNALS
CLOCK
CLOCK
W&S
SIGNALS
MULTI-
PLEXING
SIGNALS
CLOCK
SIGNAL
CONTROL SIGNAL GENERATOR
13

FIG. 4

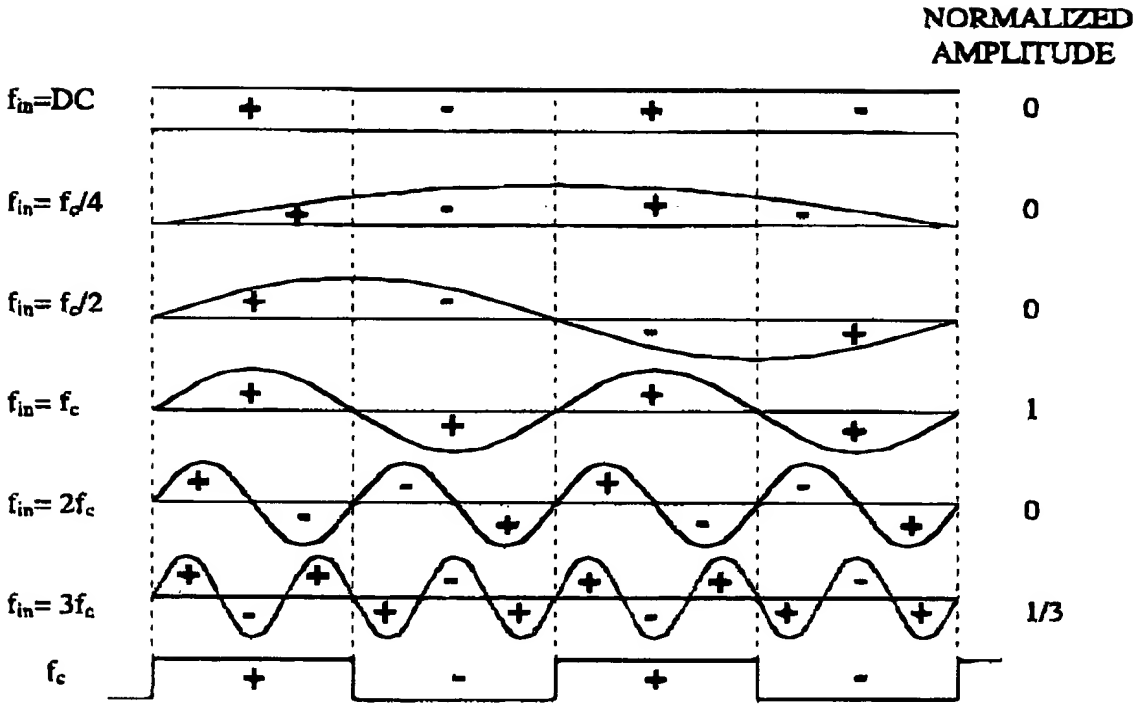

NORMALIZED AMPLITUDE
f_{in}=DC
f_{in}= f_c/4
f_{in}= f_c/2
f_{in}= f_c
f_{in}= 2f_c
f_{in}= 3f_c
f_c
0
0
0
1
0
1/3

FIG. 5

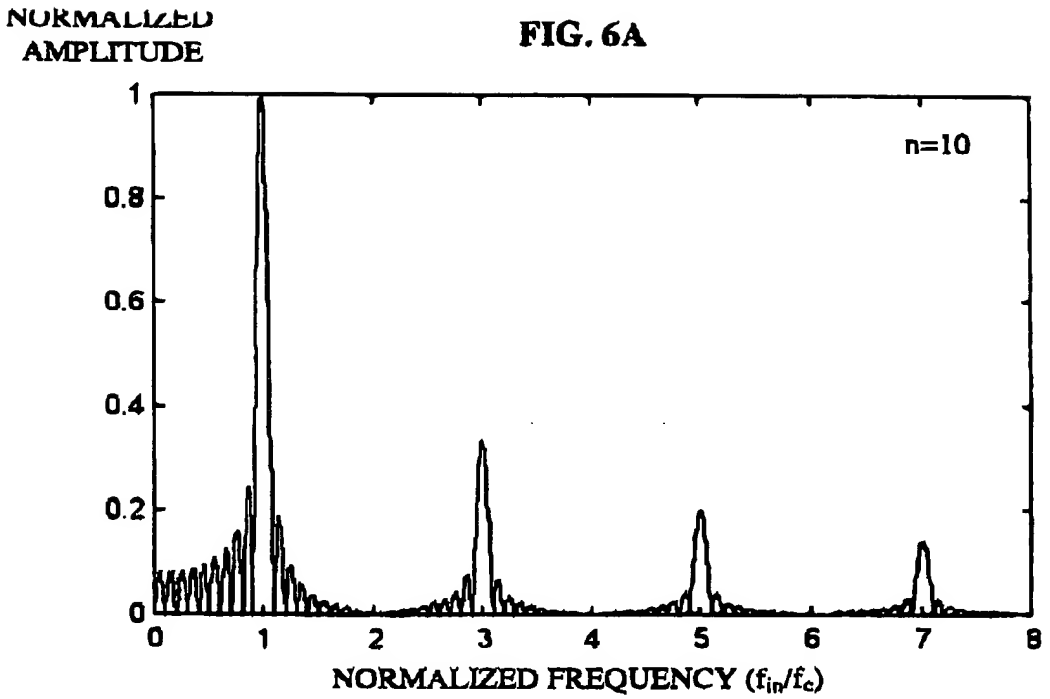
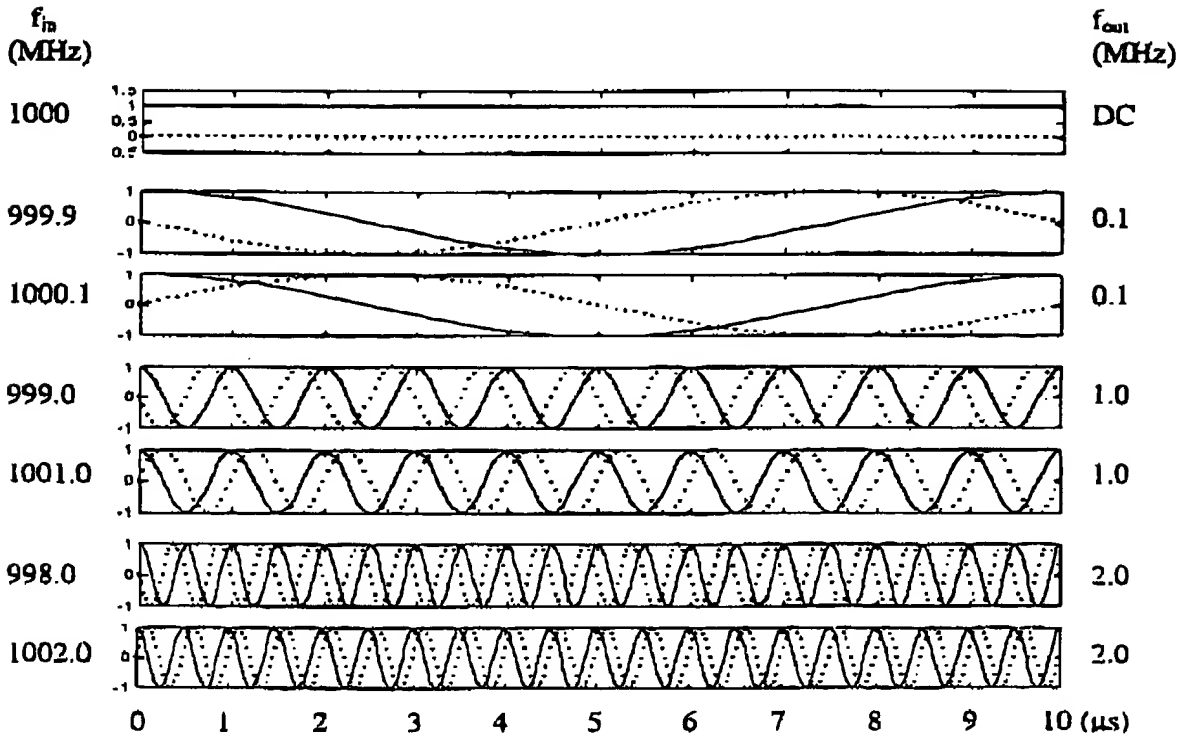


FIG. 6A



Note: 1. f_c=1000 MHz.
2. I in solid line and Q in dash line.

FIG. 6B

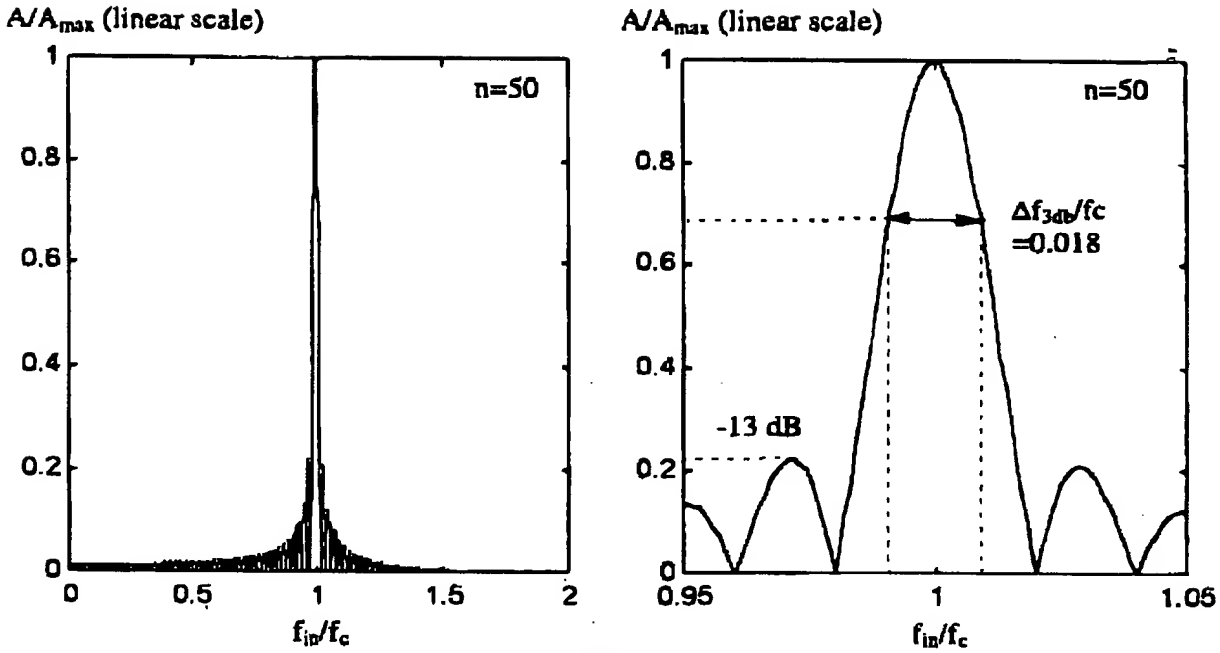

A/A_max (linear scale)
n=50
f_in/f_c
A/A_max (linear scale)
n=50
Δf_3db/fc
=0.018
-13 dB
f_in/f_c

FIG. 7A

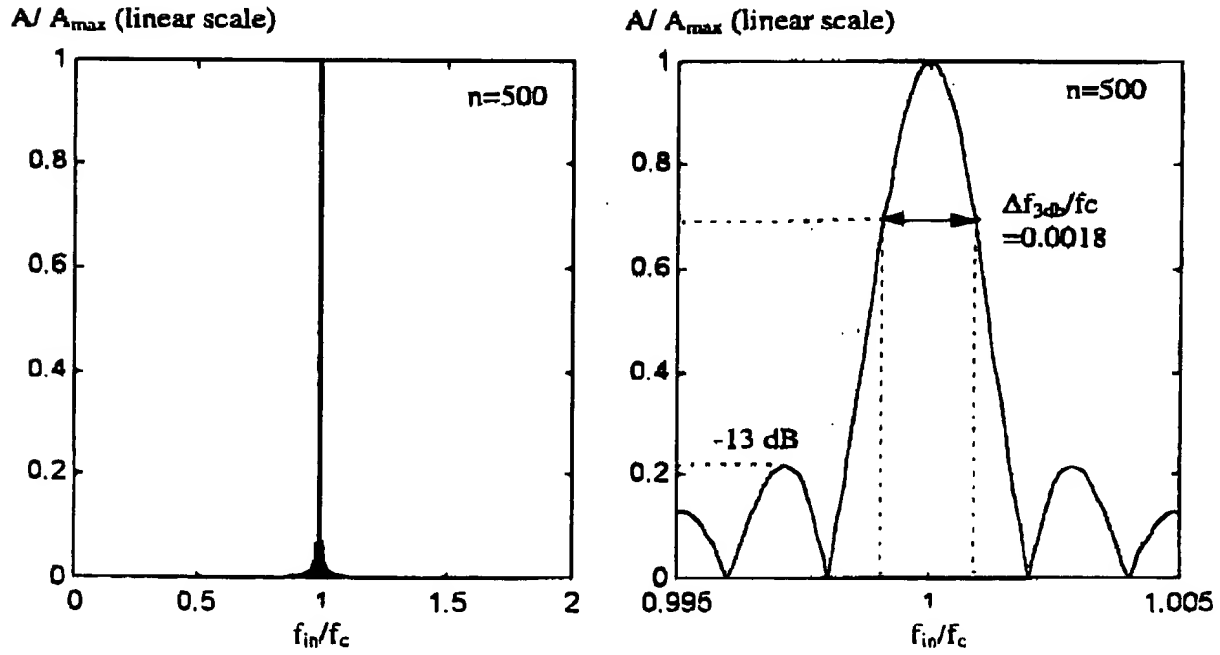

A/ A_max (linear scale)
n=500
f_in/f_c
A/ A_max (linear scale)
n=500
Δf_3db/fc
=0.0018
-13 dB
f_in/f_c

FIG. 7B

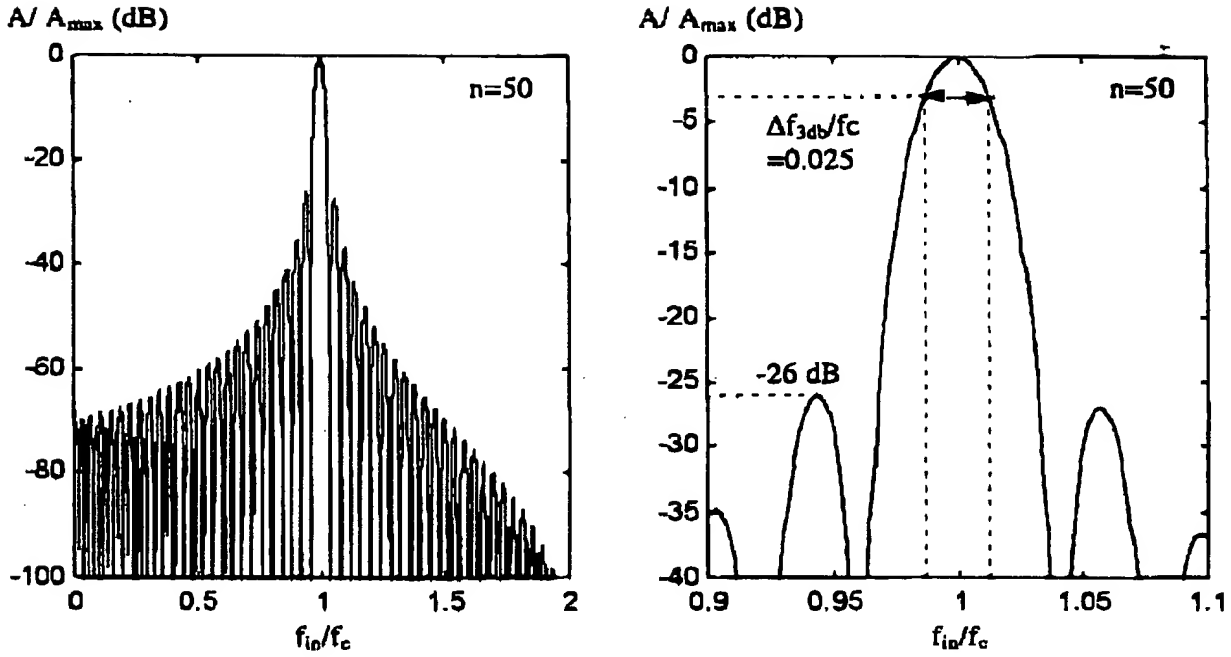

A/ Amax (dB)
n=50
fin/fc
A/ Amax (dB)
n=50
Δf3dB/fc
=0.025
-26 dB
fin/fc

FIG. 8A

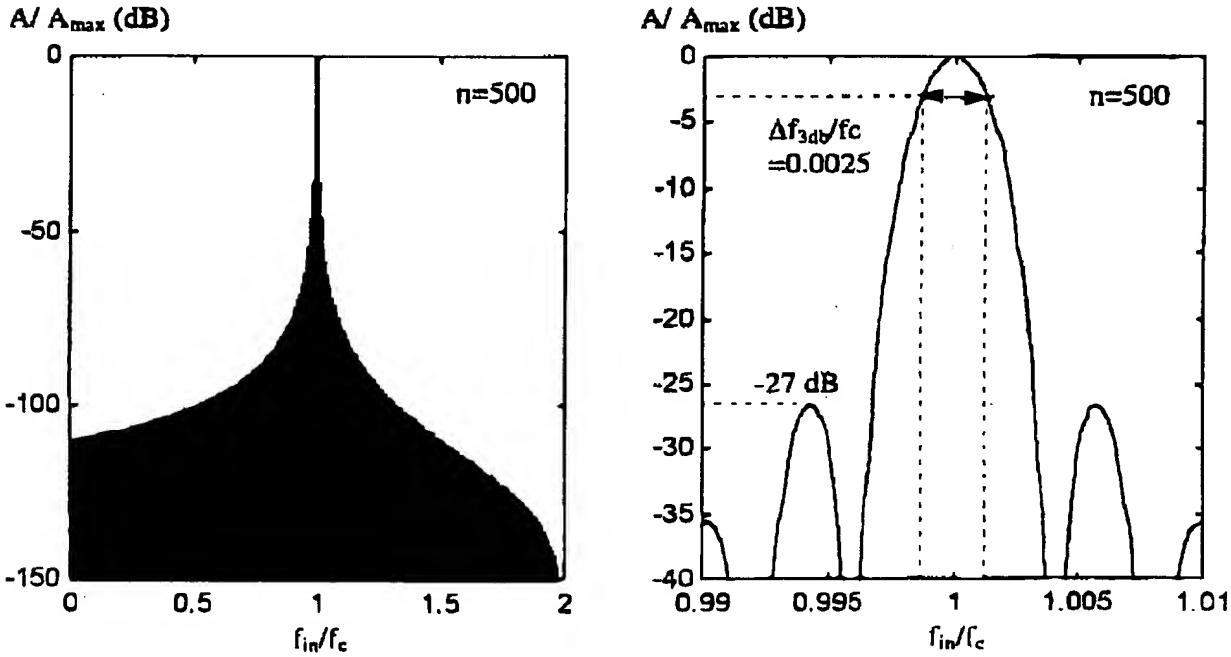

A/ Amax (dB)
n=500
fin/fc
A/ Amax (dB)
n=500
Δf3dB/fc
=0.0025
-27 dB
fin/fc

FIG. 8B

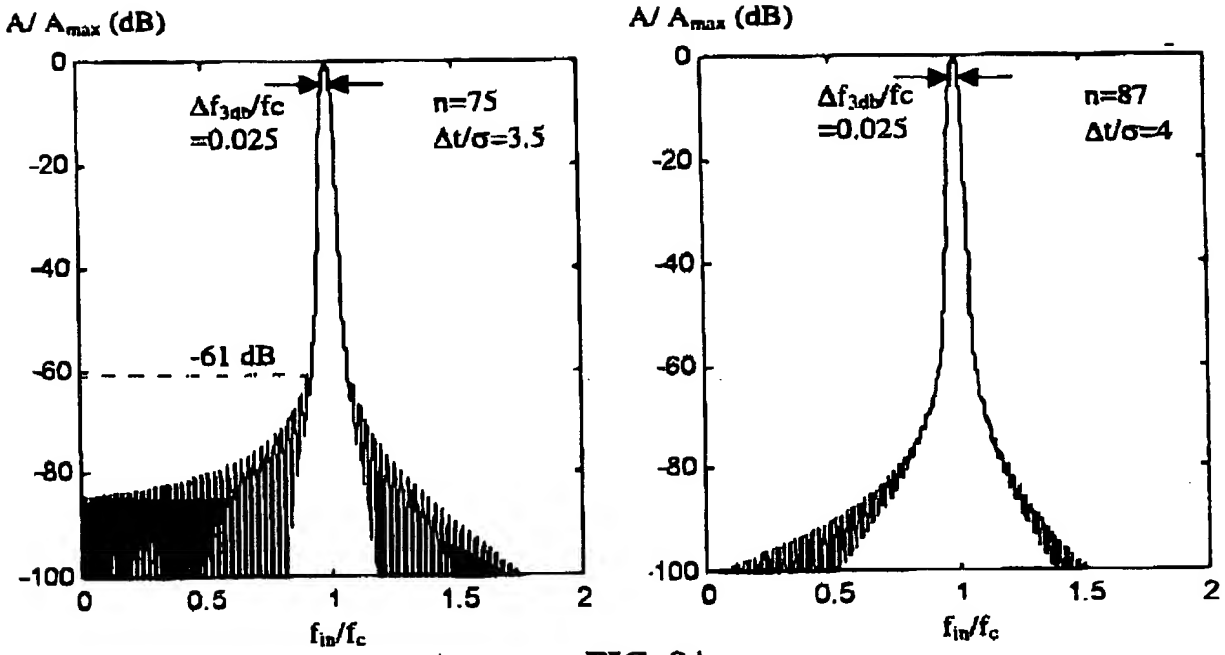

A/ Amax (dB)
Δf3db/fc
=0.025
n=75
Δt/σ=3.5
-61 dB
fin/fc
A/ Amax (dB)
Δf3db/fc
=0.025
n=87
Δt/σ=4
fin/fc

FIG. 9A

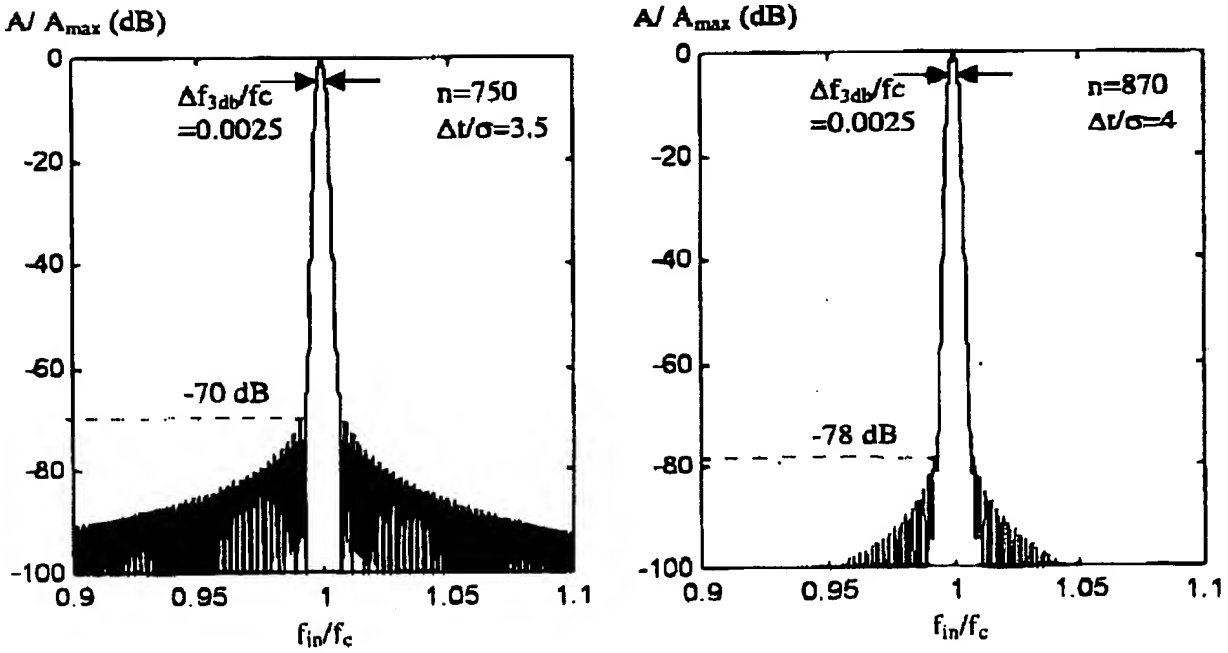

A/ Amax (dB)
Δf3db/fc
=0.0025
n=750
Δt/σ=3.5
-70 dB
fin/fc
A/ Amax (dB)
Δf3db/fc
=0.0025
n=870
Δt/σ=4
-78 dB
fin/fc

FIG. 9B

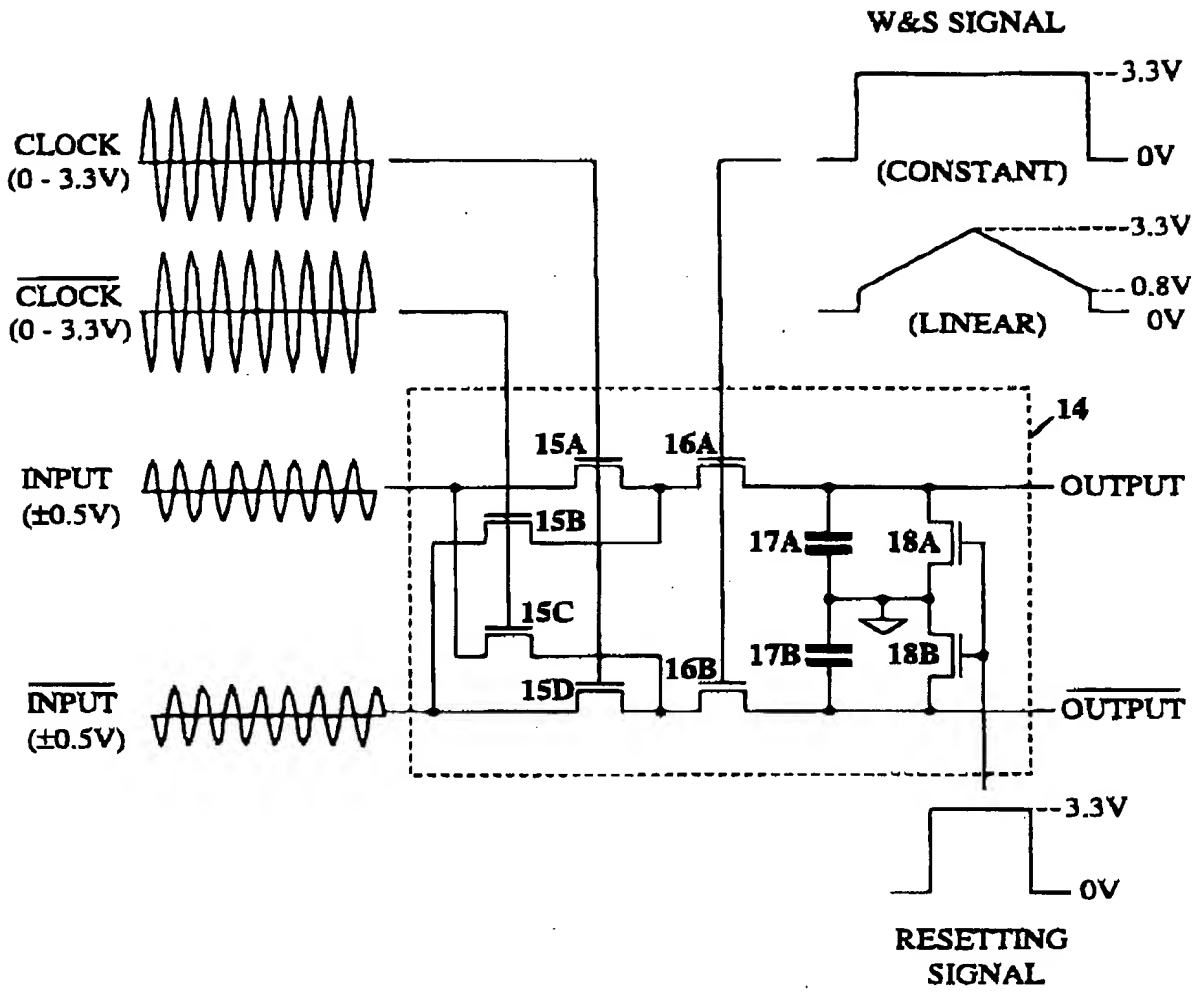

W&S SIGNAL
3.3V
0V
(CONSTANT)
3.3V
0.8V
0V
(LINEAR)
CLOCK
(0 - 3.3V)
CLOCK
(0 - 3.3V)
INPUT
(±0.5V)
INPUT
(±0.5V)
14
15A
16A
15B
15C
15D
16B
17A
18A
17B
18B
OUTPUT
OUTPUT
3.3V
0V
RESETTING
SIGNAL

FIG. 10

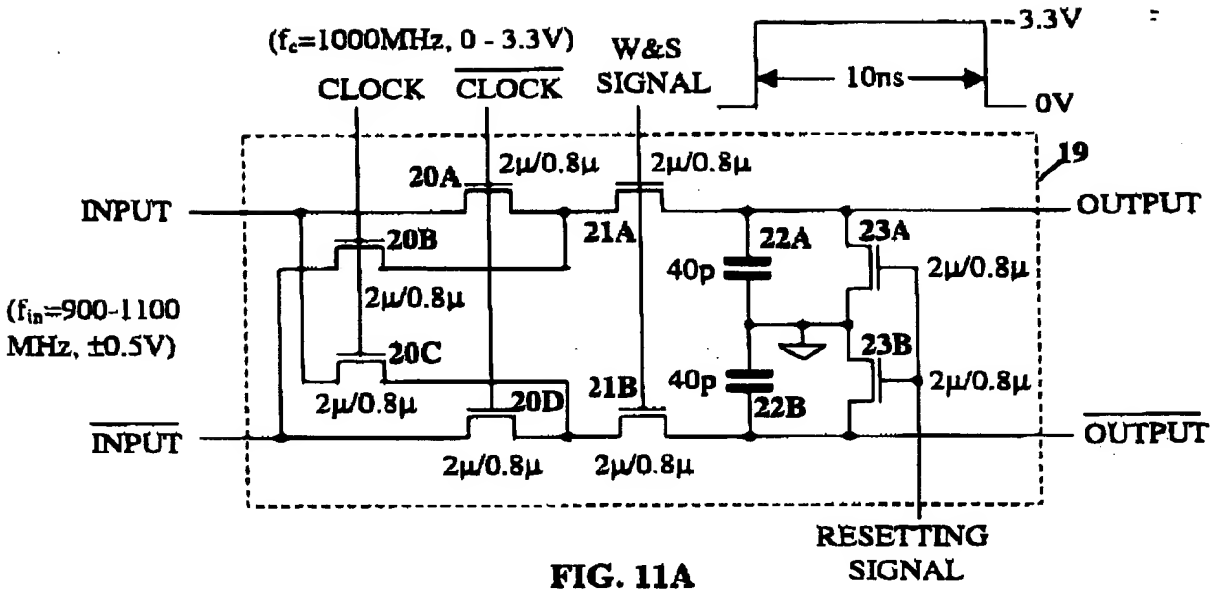
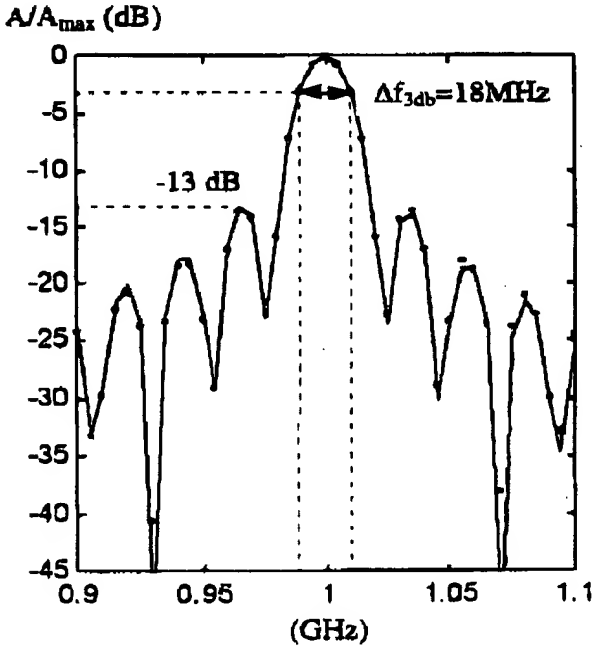


FIG. 11A



Note: 1. Ideal curve in solid line.
2. HSPICE simulation in dots.

FIG. 11B

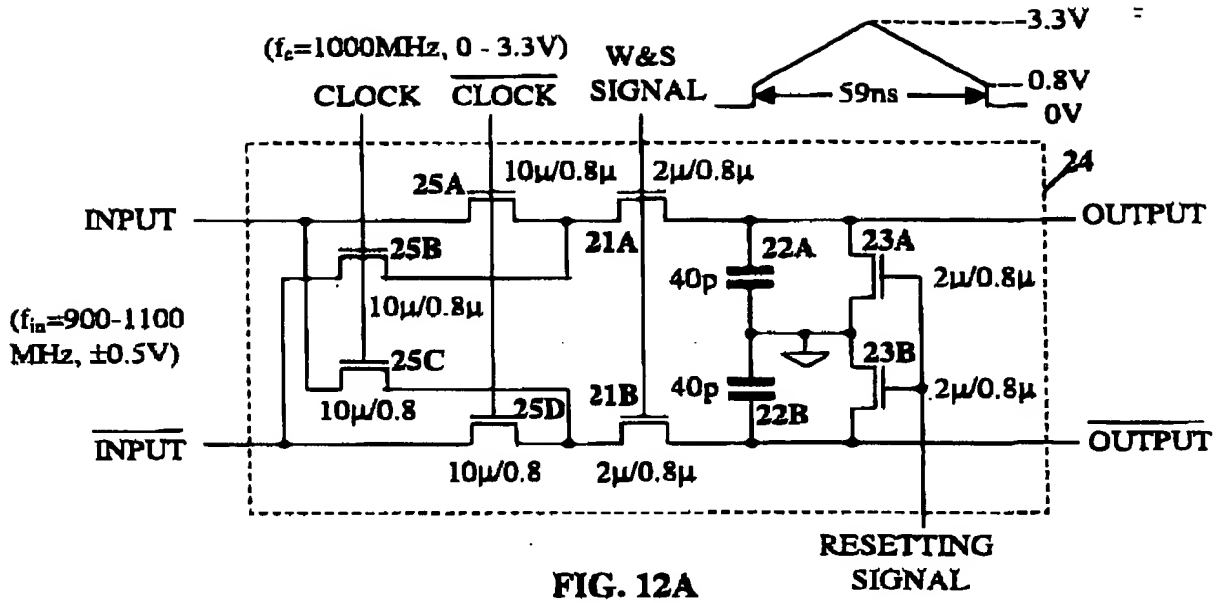
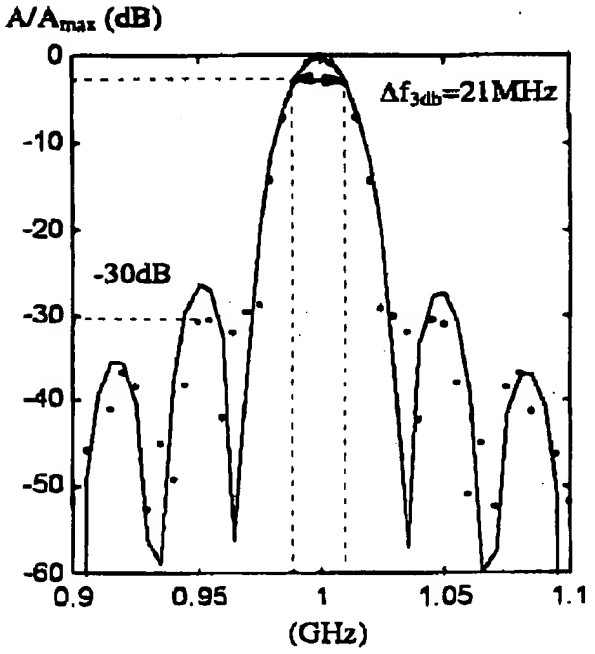


FIG. 12A



Note: 1. Ideal curve in solid line.
2. HSPICE simulation in dots.

FIG. 12B

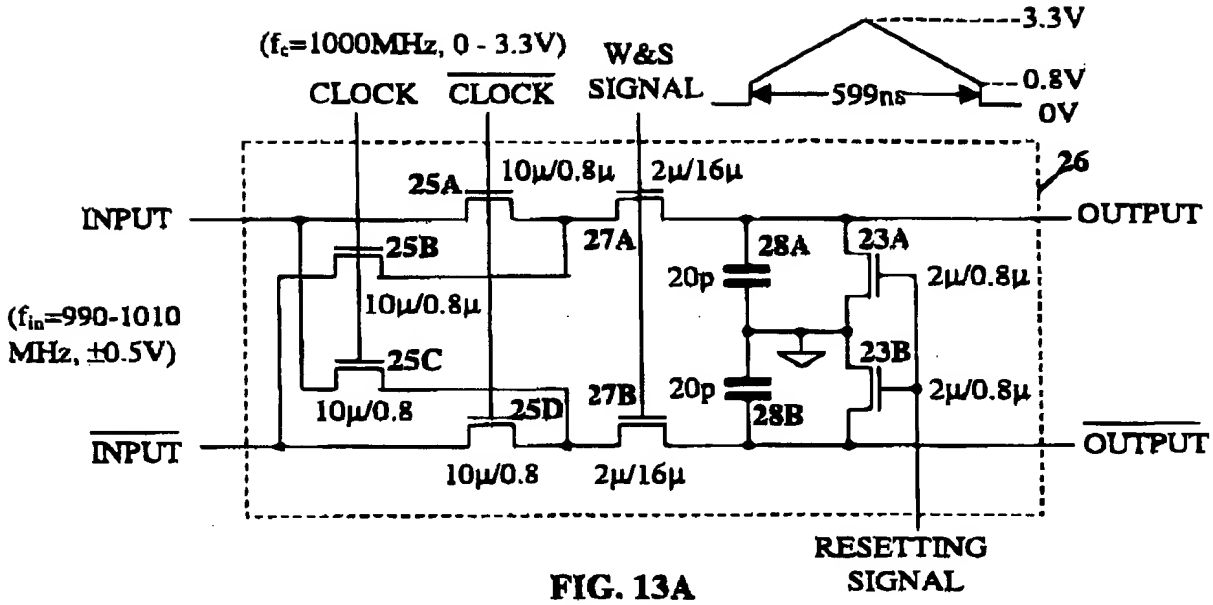
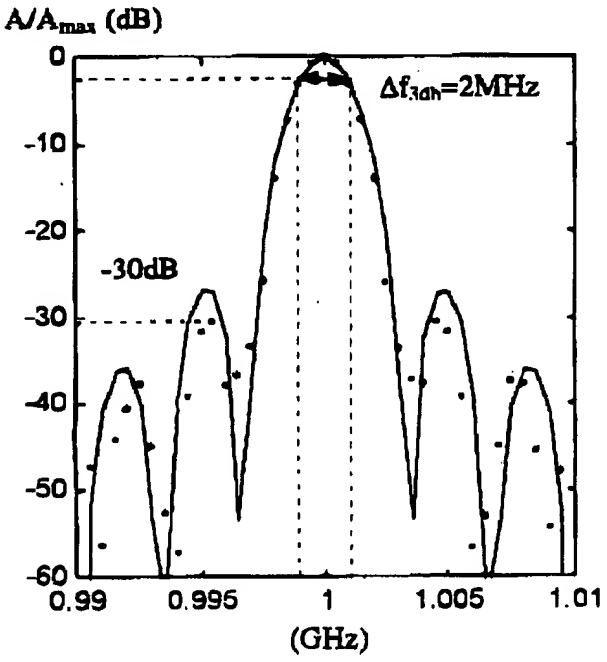


FIG. 13A



Note: 1. Ideal curve in solid line.
2. HSPICE simulation in dots.

FIG. 13B

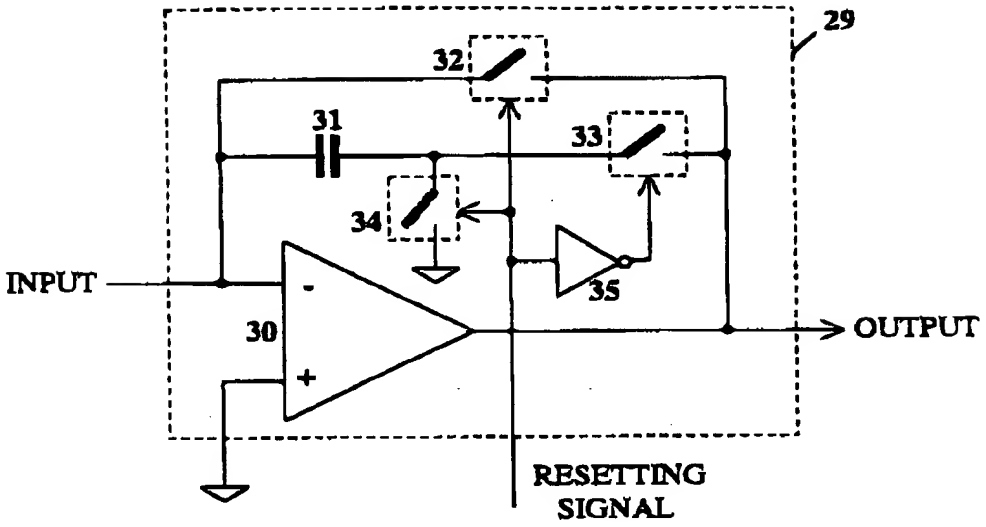


FIG. 14A

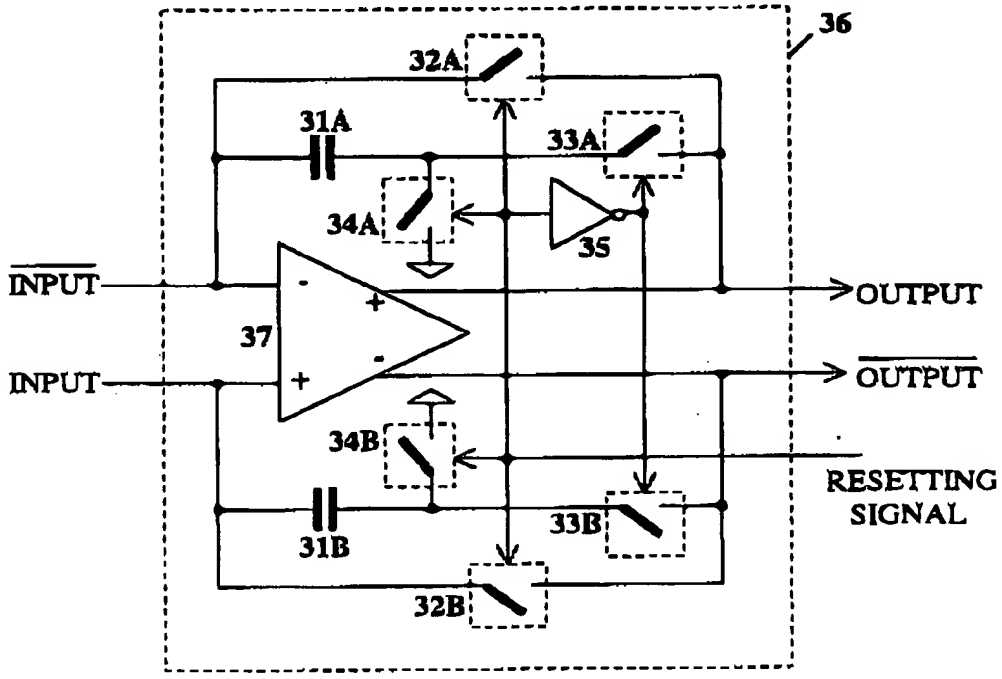


FIG. 14B

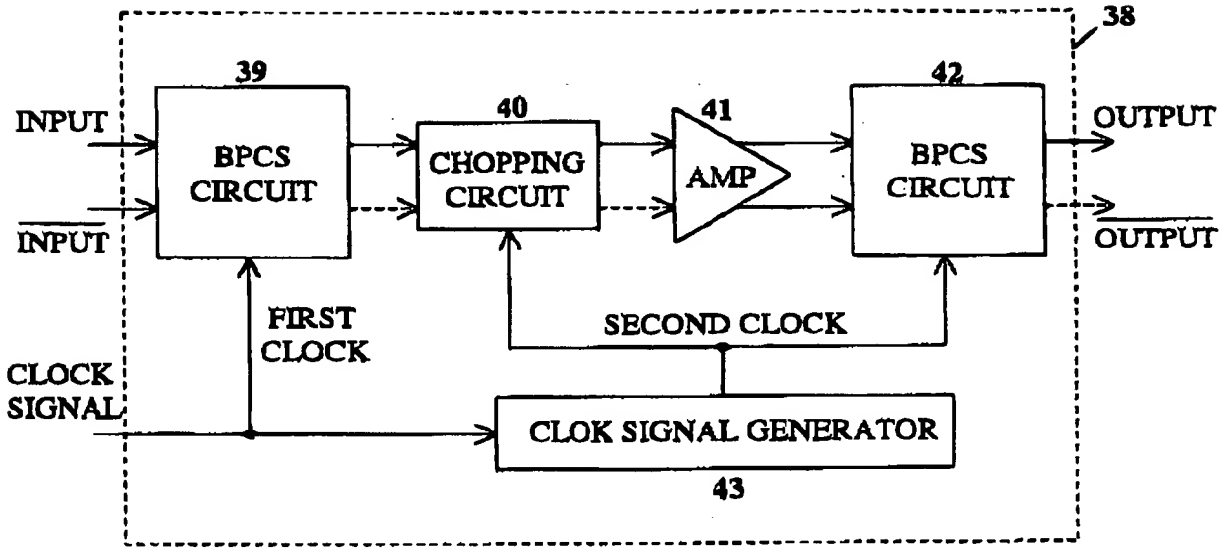

38
39
40
41
42
INPUT
INPUT
BPCS CIRCUIT
CHOPPING CIRCUIT
AMP
BPCS CIRCUIT
OUTPUT
OUTPUT
FIRST CLOCK
SECOND CLOCK
CLOCK SIGNAL
CLOK SIGNAL GENERATOR
43

FIG. 15

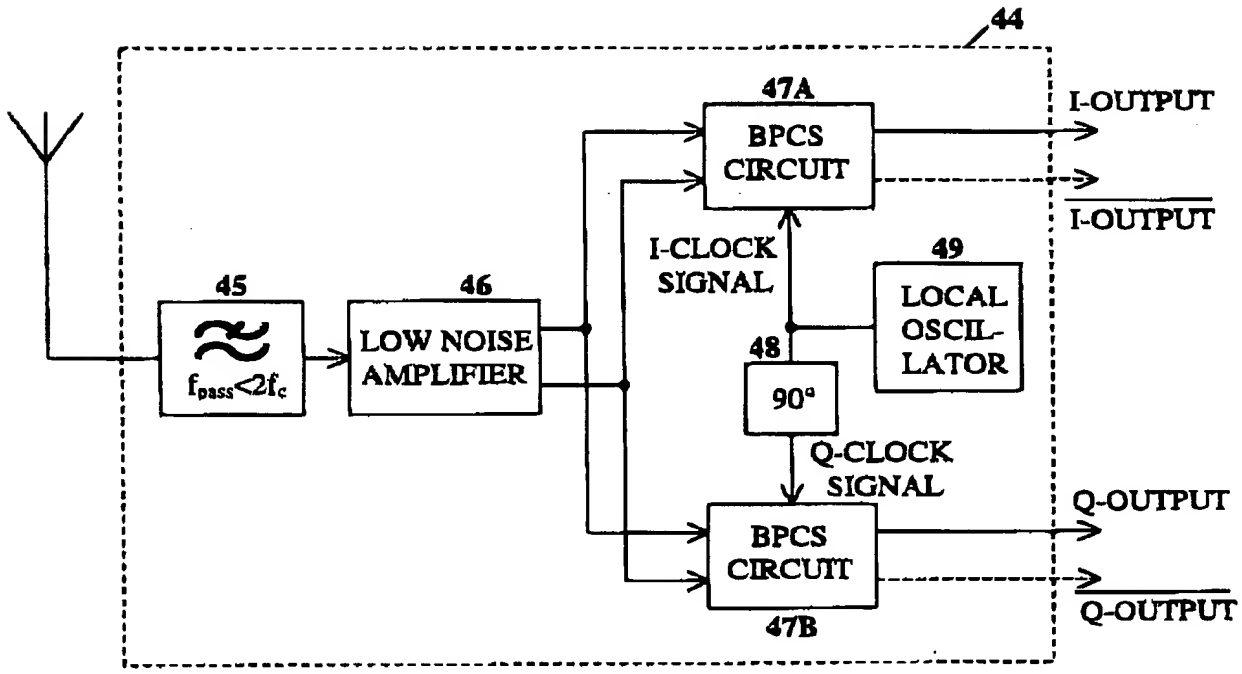

44
47A
BPCS CIRCUIT
I-OUTPUT
$\overline{\text{I-OUTPUT}}$
I-CLOCK SIGNAL
49
LOCAL OSCIL-LATOR
45
$f_{pass}<2f_c$
46
LOW NOISE AMPLIFIER
48
90°
Q-CLOCK SIGNAL
Q-OUTPUT
BPCS CIRCUIT
$\overline{\text{Q-OUTPUT}}$
47B

FIG. 16